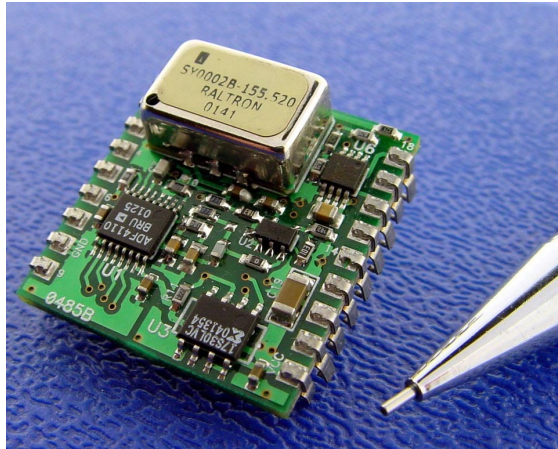


SY02-HIPL

Date: January 6, 2004



- **INTRODUCTION**

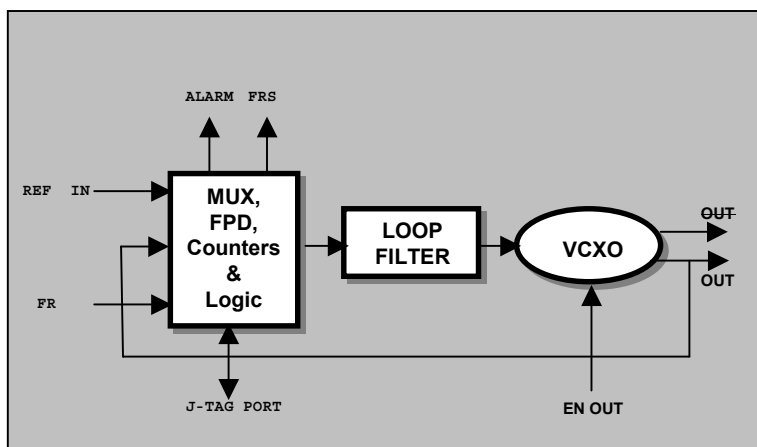
The SY02-HIPL is a high frequency crystal-based PLL synchronizer designed as a module level subsystem for easy incorporation into telecommunication equipment.

- **FEATURES**

- Low jitter output from intrinsically low jitter VCXO or VCSO;
- One references LVEPECL input **up to 800MHz** (pre-select frequency value –upon order)
- One high frequency LVPECL output **up to 800MHz** with E/D function (pre-select frequency value –upon order)
- Alarms and status;
- Provides free running clock output;
- The unit changes timing modes in response to external events;
- J-TAG service port for re-programming and servicing;
- 3.3V DC power supply
- Small dimensions: 0.96" x 1.050"

- **APPLICATIONS**

- ATM
- SDH
- PDH
- SONET
- Other telecommunication equipment.



• DESCRIPTION

The SY02-HIPL is a High Frequency Phase Lock Loop has been designed as a module level subsystem for easy incorporation into telecommunication equipment. The module generates the high frequency (up to 622.08MHz) output from a low jitter VCXO (Crystal Based Oscillator) or VCXO (SAW based oscillators). The output can be disabled externally by setting OUTEN pin high. The SY02-HIPL can be locked to one reference input frequency of 155.52MHz. The module has fast locking time and tolerates reference inputs with different duty cycles. The loop bandwidth is optimized according to used VCXO and wanted output performance. The ALARM output signals monitor the status of the phase loop LOL (Loss of Lock) and LOR (Loss of Reference). If the reference REF IN is absent, the SY02-HIPL will automatically switch to free run mode and FRS output will indicate it. The SMD package dimensions are 0.96x1.050 inch and power supply is 3.3V.

- OUTPUT PROGRAMMING

OUTEN	FR	OUTPUT
0	0	Locked to Reference
1	X	Output Disabled
0	1	Free-Run

- ALARM STATES

LOL	LOR	ALARM
0	0	No alarm
1	0	1
0	1	1

• **PIN DESCRIPTION**

	Name	Description	Signal Technology	VL			VH/ DC Voltage		
				Min	Typ	Max	Min	Typ	Max
1	ENABLE	Output Enable -> the input pin to enable the output, active low	DC	0	0.15	0.3	2.97	3.3	3.465
2	TCK	J-TAG port for factory usage – TCK	----	----	----	----	----	----	----
3	TDO	J-TAG port for factory usage – TDO	----	----	----	----	----	----	----
4	REFA IN	Reference A Input -> Reference A input signal	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.560	Vcc-1.085	Vcc-1.025	Vcc-0.885
5	SEL	Select Input Reference -> input to select A (SEL=0) or B (SEL=1)	DC	0	0.15	0.3	2.97	3.3	3.465
6	RESET	Reset input -> Reset active high In normal operation must be Grounded	DC	0	0.15	0.3	2.97	3.3	3.465
7	REFB IN	Reference B Input -> Reference B input signal	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.560	Vcc-1.085	Vcc-1.025	Vcc-0.885
8	GND	Ground	----	----	----	----	----	----	----
9	FRS	Free-Run Status -> Output indicates that the module is in free run, active high	DC	0	0.15	0.3	2.97	3.3	3.465
10	Vcc	Positive supply voltage	DC	----	----	----	3.135	3.3	3.465
11	NC	Not Connected	----	----	----	----	----	----	----
12	ALARM	Alarm out -> Alarm output indicates loss of reference or loss of lock – High when the unit is Unlocked	DC	0	0.15	0.3	2.97	3.3	3.465
13	FR	Free-Run -> Control input to select free run of the module, active high	DC	0	0.15	0.3	2.97	3.3	3.465
14	TDI	J-TAG port for factory usage – TDI	----	----	----	----	----	----	----
15	TMS	J-TAG port for factory usage – TMS	----	----	----	----	----	----	----
16	OUT	Oscillator Output -> Output of the module	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.560	Vcc-1.085	Vcc-1.025	Vcc-0.885
17	GND	Ground	----	----	----	----	----	----	----
18	OUT	Complimentary Output	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.560	Vcc-1.085	Vcc-1.025	Vcc-0.885

• **ORDERING INFORMATION**

- Input/Output Frequencies available;

Frequency	Suffix	Frequency	Suffix	Frequency	Suffix
19.440MHz	O1**	112.000MHz	B7	777.6000MHz	F6
20.000MHz	M1**	114.000MHz	B8		
20.1416MHz	A3**	125.000MHz	G2		
20.4800MHz	A4**	133.000MHz	G4		
22.2171MHz	A5**	139.264MHz	E6		
26.0000MHz	G3**	155.520MHz	O4		
27.0000MHz	A6**	156.250MHz	G6		
29.4912MHz	A7**	161.1328MHz	B9		
32.768MHz	E5**	166.6286MHz	B10		
34.560MHz	A8**	167.3316MHz	C1		
37.0560MHz	A9**	168.0407MHz	C2		
38.880MHz	O2**	175.0000MHz	C3		
44.4343MHz	B1**	178.9440MHz	C4		
44.7360MHz	T3**	184.3200MHz	C5		
51.8400MHz	D2**	311.0400MHz	O6		
61.4400MHz	U1**	622.0800MHz	O7		
62.5000MHz	G5**	625.000MHz	C8		
65.5360MHz	B2**	644.5312MHz	C9		
77.7600MHz	O3	666.5143MHz	C10		
78.125MHz	B3	669.1281MHz	F1		
78.6432MHz	B4	669.3266MHz	F2		
82.9440MHz	B5	690.5692MHz	F3		
92.6000MHz	U3	710.9486MHz	F4		
100.000MHz	B6	719.7344MHz	F5		

** Signifies an Input Frequency Only

➤ P/N System

SY02-HIPL – < Input Frequency > - < Output Frequency > - S - < Temp. Range > - < Cover Option >

➤ See above Chart
If not listed Place **NL** and state the Freq.)

➤ See above Chart
(If Output Freq. Not applied place **NA** and state the Freq.)

➤ Supply Voltage;
4 – 3.3V

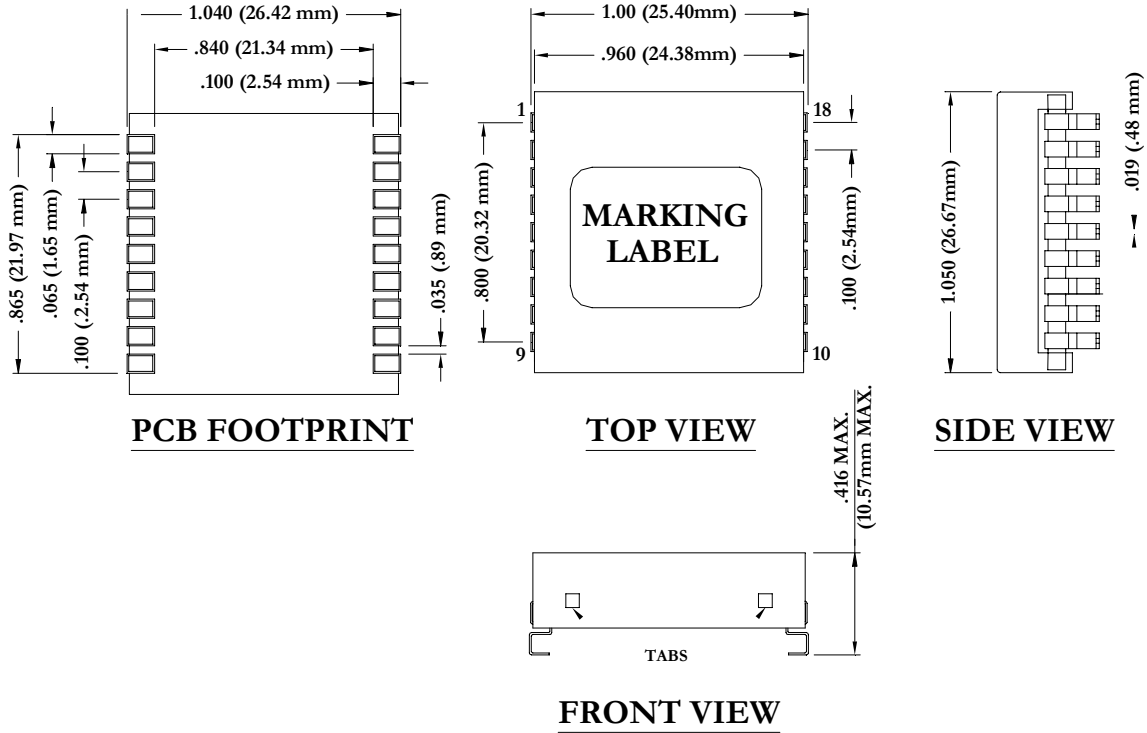
➤ Operating Temperature Range;
C - 0°C to 70°C
I -40°C to +85°C

➤ Cover Option;
M – Metal Cover
N - Non Covered unit

● SPECIFICATION

General Specifications	Mechanical	0.96" x 1.050"	SMT Module FR4 18 pins dual-in-line
	Power Environment	3.3VDC, <200mA Operating Temperature Humidity	Regulated 0°C to 70°C 5% to 95% non-condensing Depend of the frequency
	Internal Oscillators	VCXO or VCXO	
Input Signals	Number of Reference Inputs	1	
	Input reference frequency	See above table	
	Signal Level	LVPECL	Voh; 2.272V min ; Vol; 1.68Vmax
Output Signals	Number of Outputs	1	
	Output 1	See above table	other frequency contact Raltron
	Output 1 Signal Level	LVPECL (W/ Complimentary option)	Voh; 2.272V min ; Vol; 1.68Vmax
	Duty Cycle	50+/-10%	50%+/-5% available upon request
	Tracking/Capture Range	±50ppm APR min	
	Free Run stability	±30ppm (VCXO) ±150PPM(VCXO)	T=+25C; Vcc/load=nominal
Signal Quality Performance	Jitter generation	<0.001UI RMS <0.001UI RMS <0.0001 UI RMS <0.0001 UI RMS	HPF 30Hz HPF 500Hz HPF 12KHz HPF 100KHz
	Jitter attenuation	-40dB -10dB	Fj=10Hz~1KHz Fj=1KHz~10MHz
	Jitter tolerance	2 μs, 10 Hz (0.05 UI @ 8KHz)	

• **OUTLINE DRAWING**



• **REFLOW PROFILE**

